Please replace the abstract with the following amended abstract:

A ferroelectric memory device includes a bit line pair, a plurality of memory cells which include one transistor and one ferroelectric capacitor, and a plurality of judgement memory cells which include two transistors and two ferroelectric capacitors. Each of the memory cells is connected to one of the bit lines of the bit line pair, and each of the judgement memory cells is connected to both of the bit lines of the bit line pair.